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A cross-sectional view of a semiconductor device 11. The device includes a substrate 13 with a trench 14. A gate stack 20A is formed on the substrate, consisting of a gate dielectric 25 and a gate electrode 21A. A source/drain region 21A is formed in the substrate, and a source/drain contact 27 is formed on top of it. The device also includes a passivation layer 26, a protective layer 22A, and a contact pad 24. The device is formed on a substrate 15.

FIG.2B

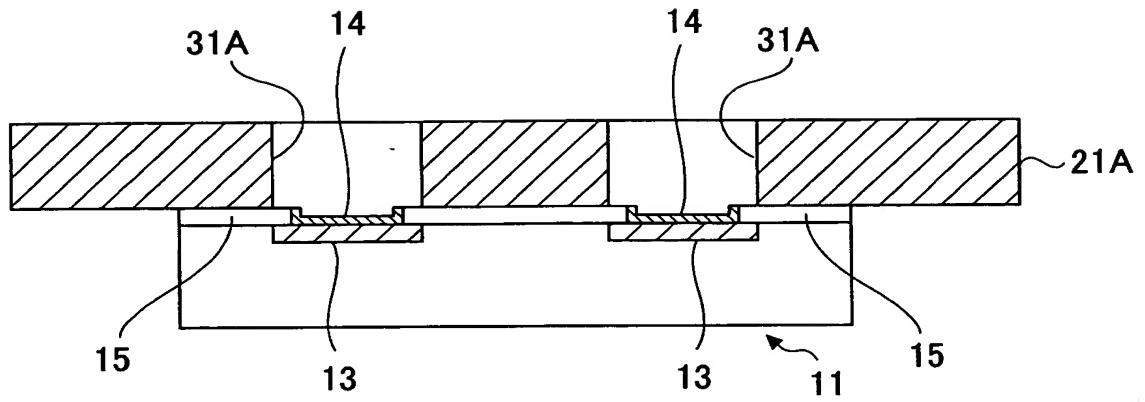


FIG.2C

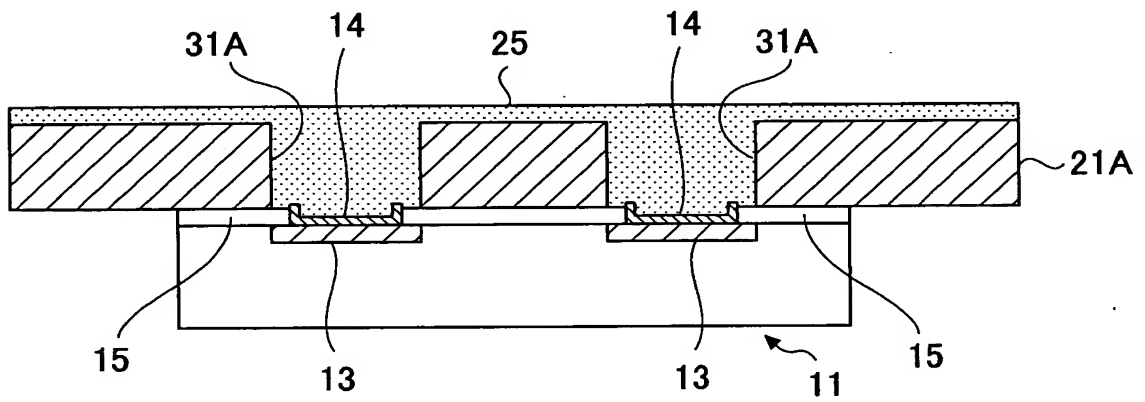


FIG.3A

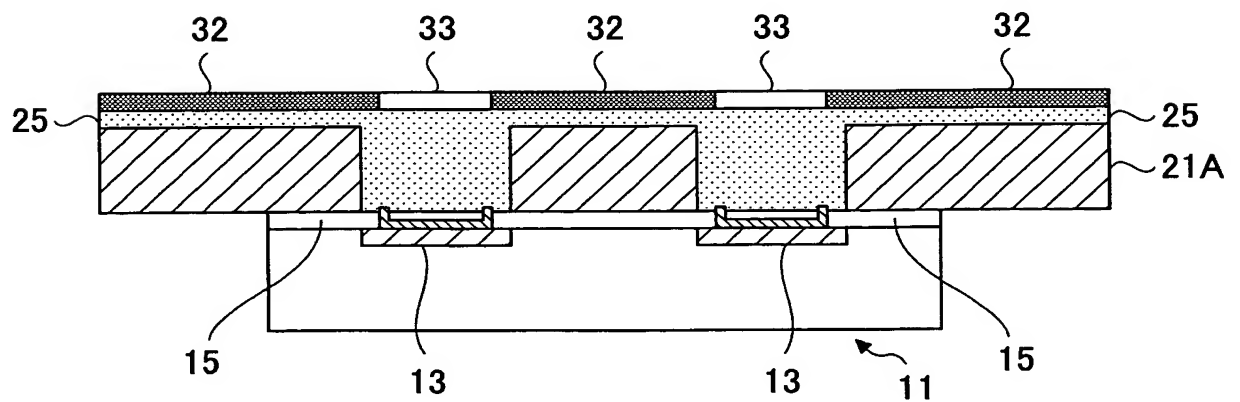


FIG.3B

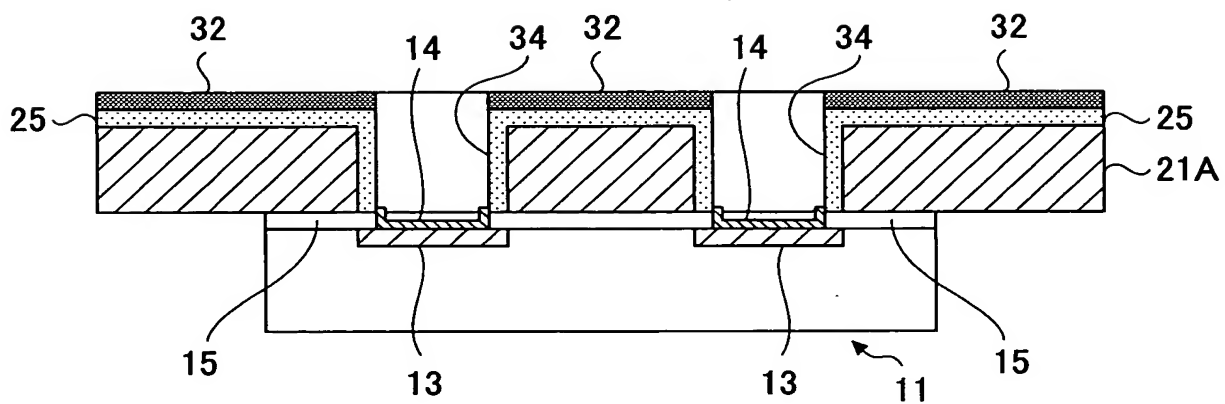


FIG.3C

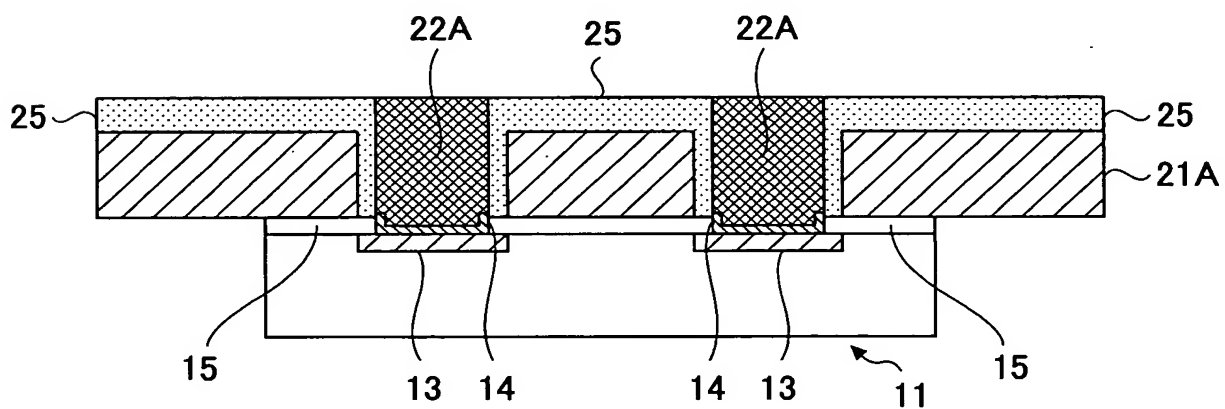


FIG.4A

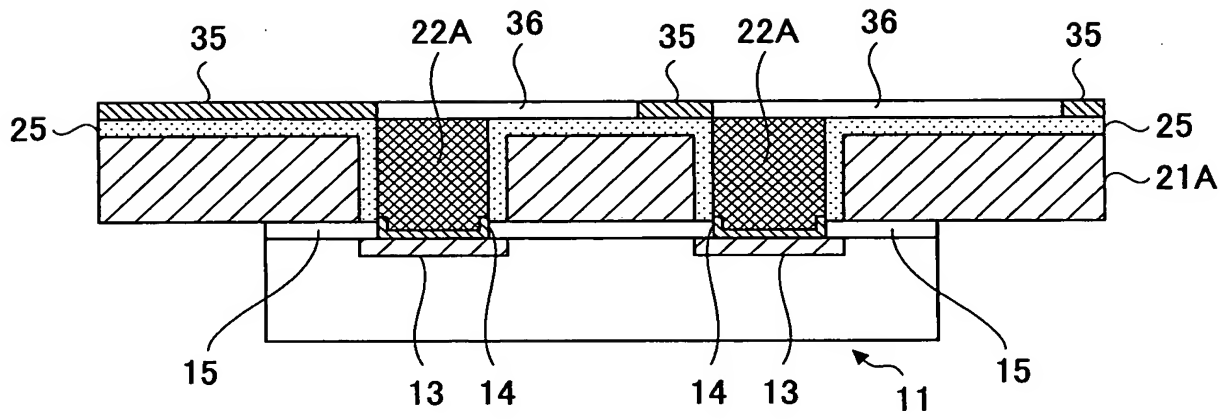


FIG.4B

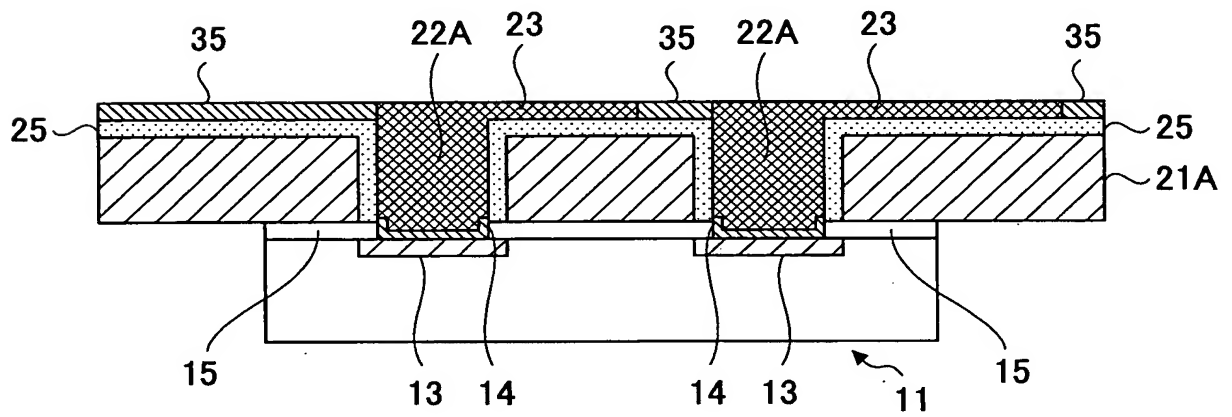


FIG.4C

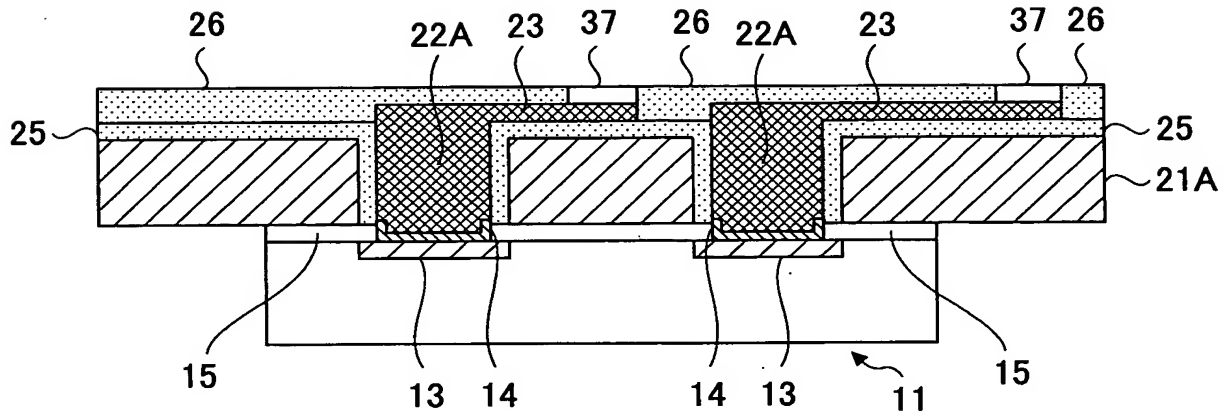


FIG.4D

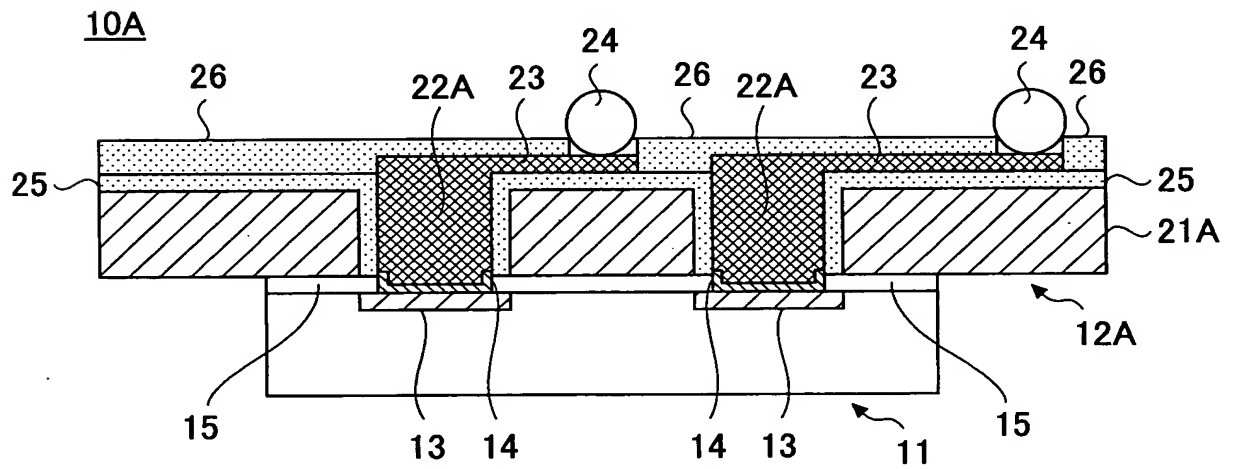


FIG.5

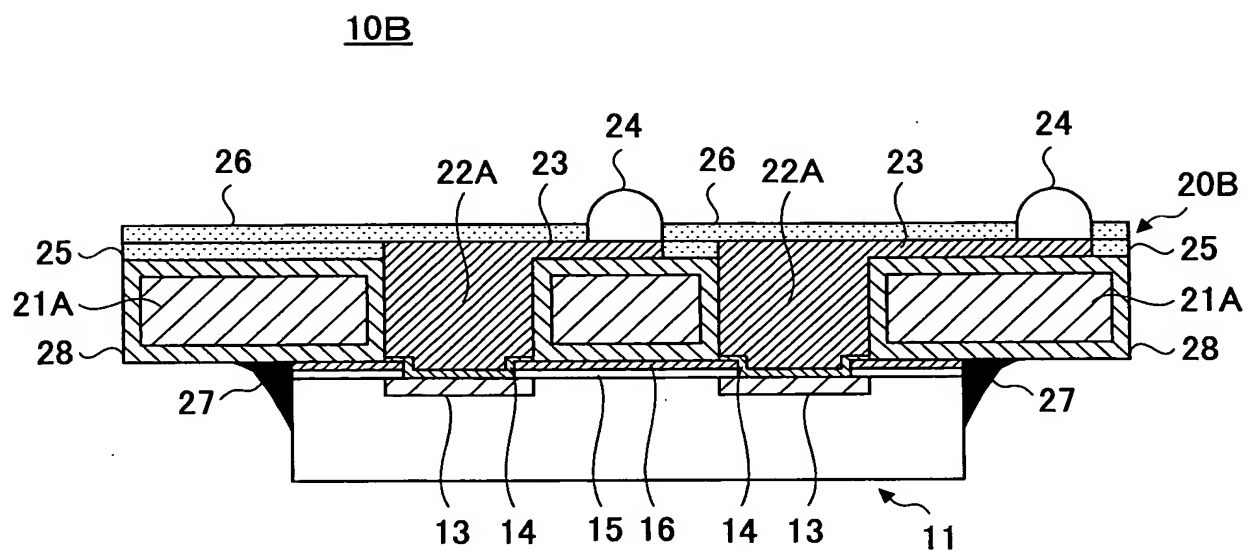


FIG.6A

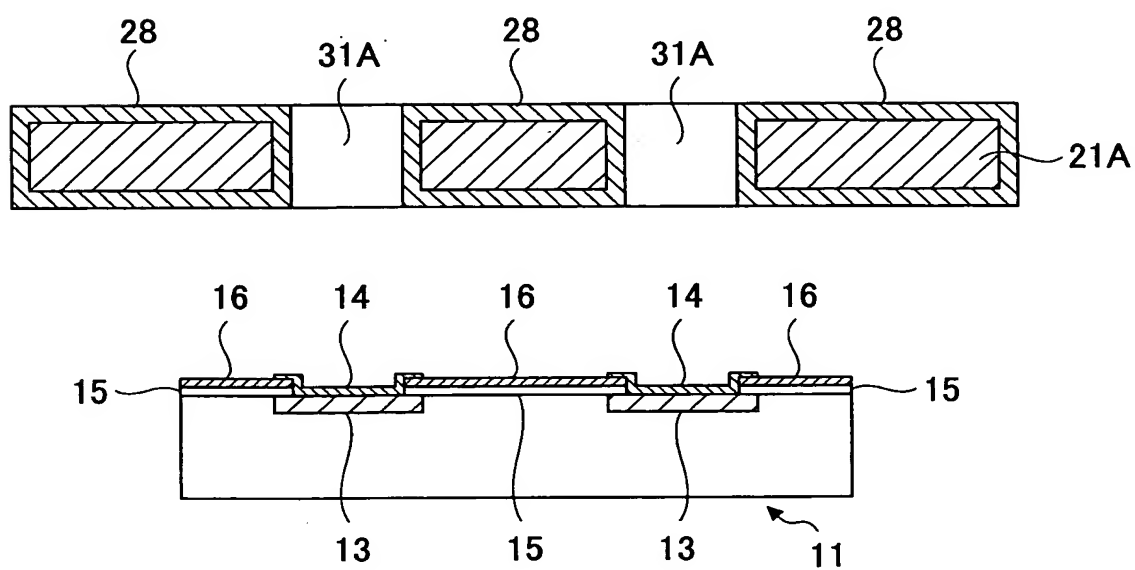


FIG.6B

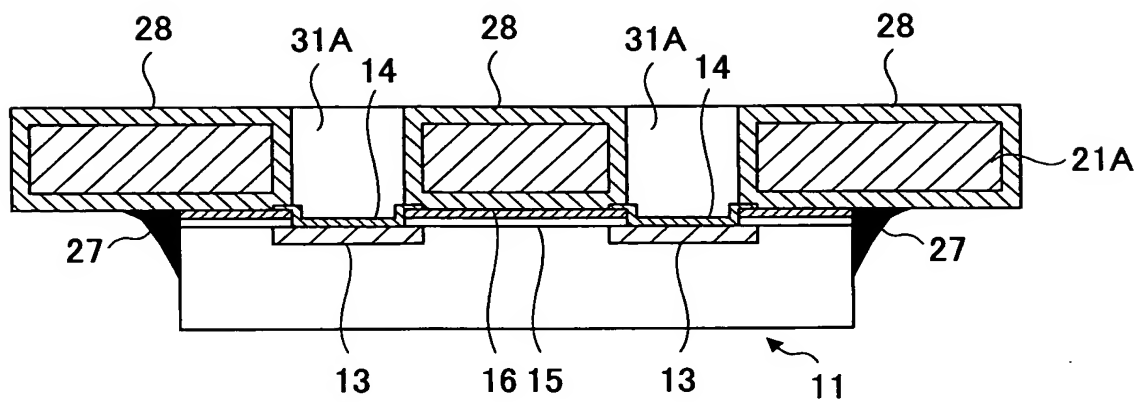


FIG.7

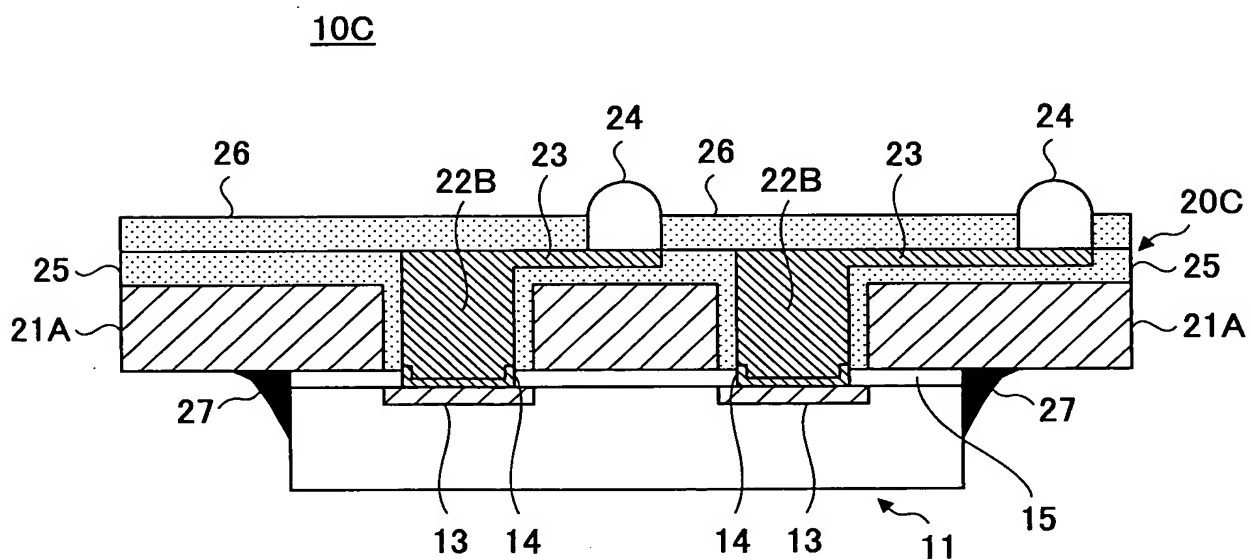


FIG.8A

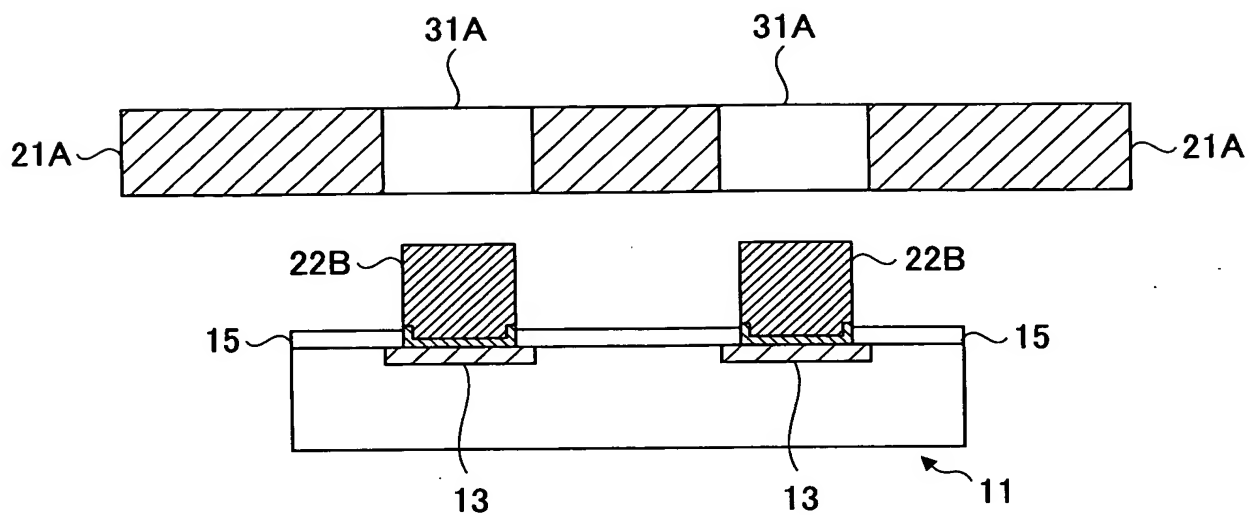


FIG.8B

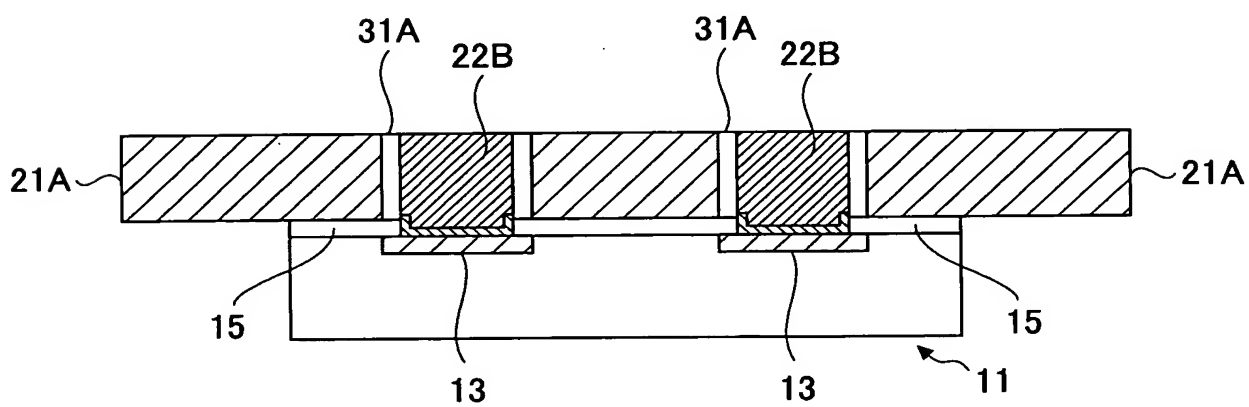


FIG.8C

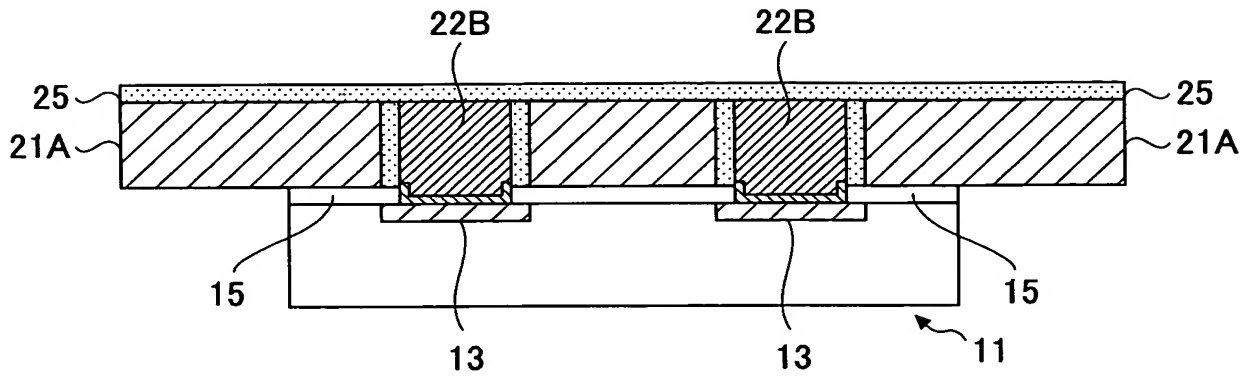


FIG.9

10D

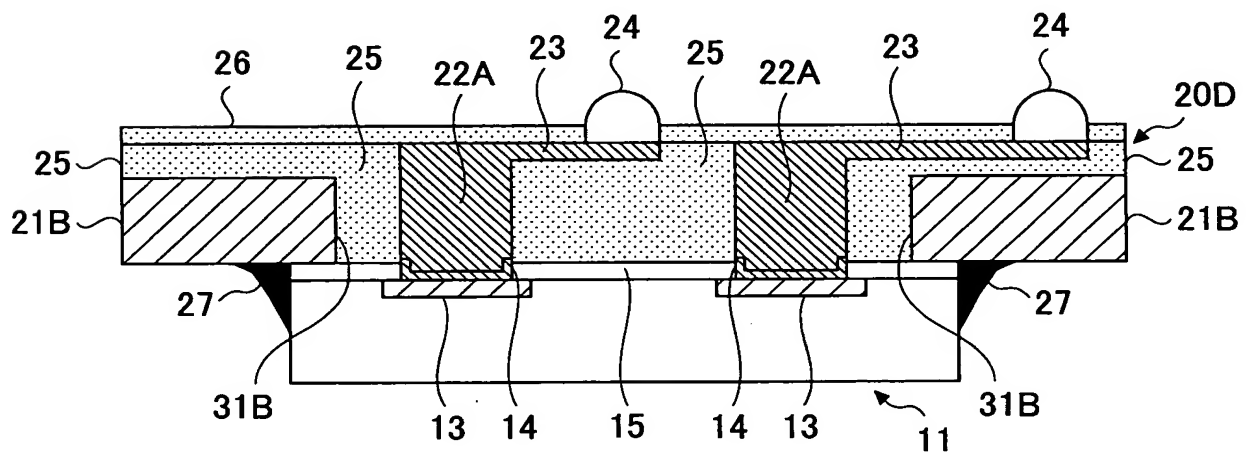


FIG.10A

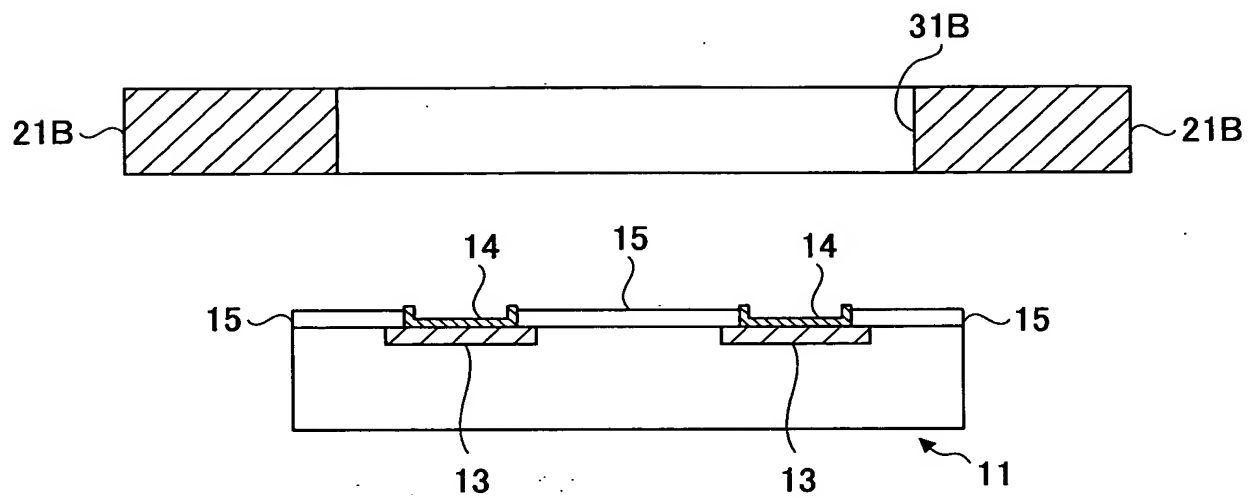


FIG.10B

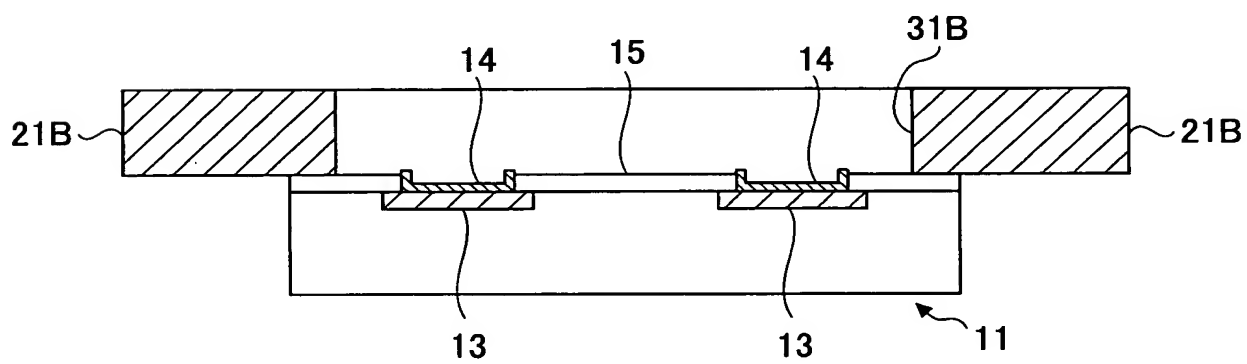


FIG.11

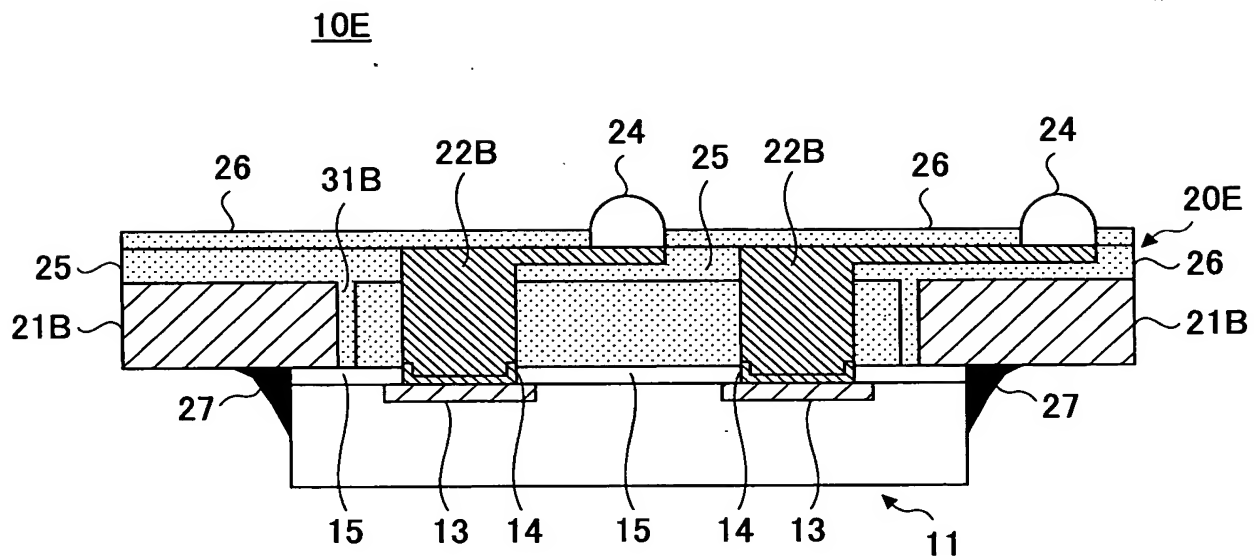
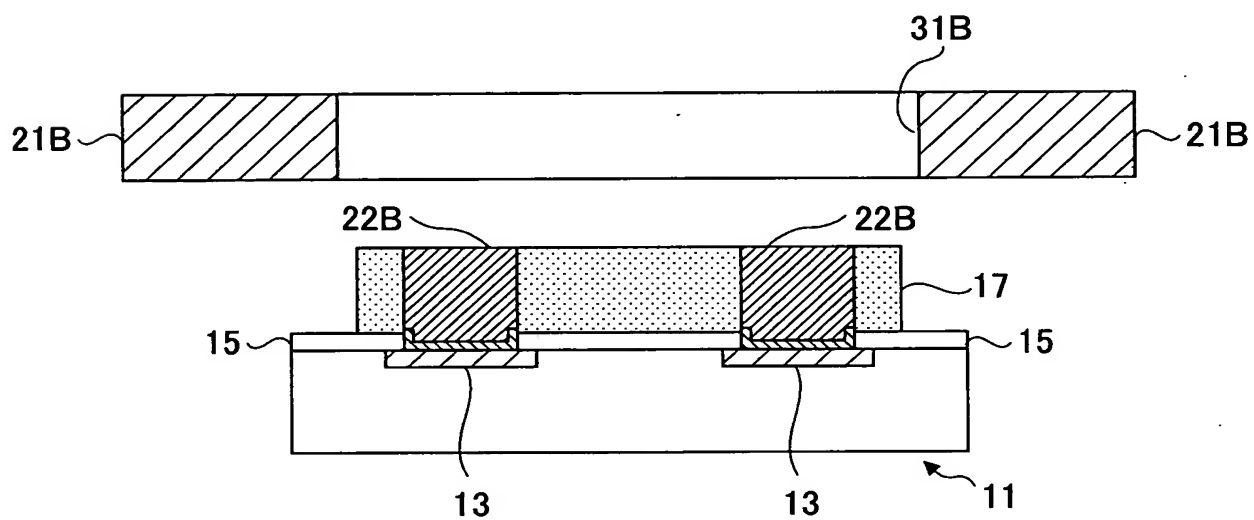


FIG.12A



A cross-sectional view of a semiconductor device 11. The device features a substrate 15 with two raised regions 13. A central layer 17 is positioned above the substrate. On either side of the central layer 17, there are regions 22B and 31B. The outermost regions are labeled 21B. The device is shown in a cross-sectional view, with the substrate 15 at the base and the various layers and regions extending upwards.

FIG.13

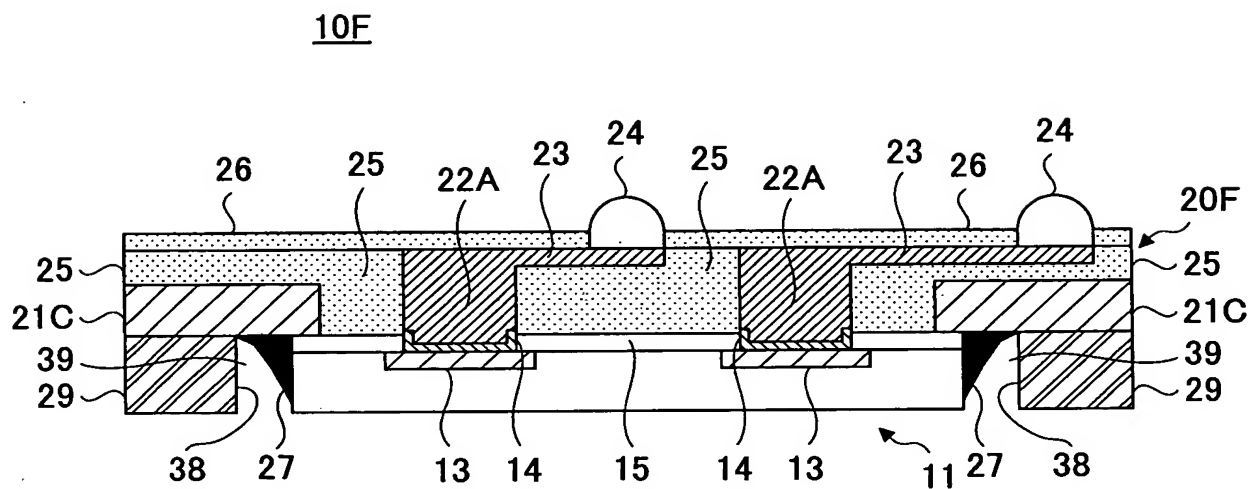


FIG.14

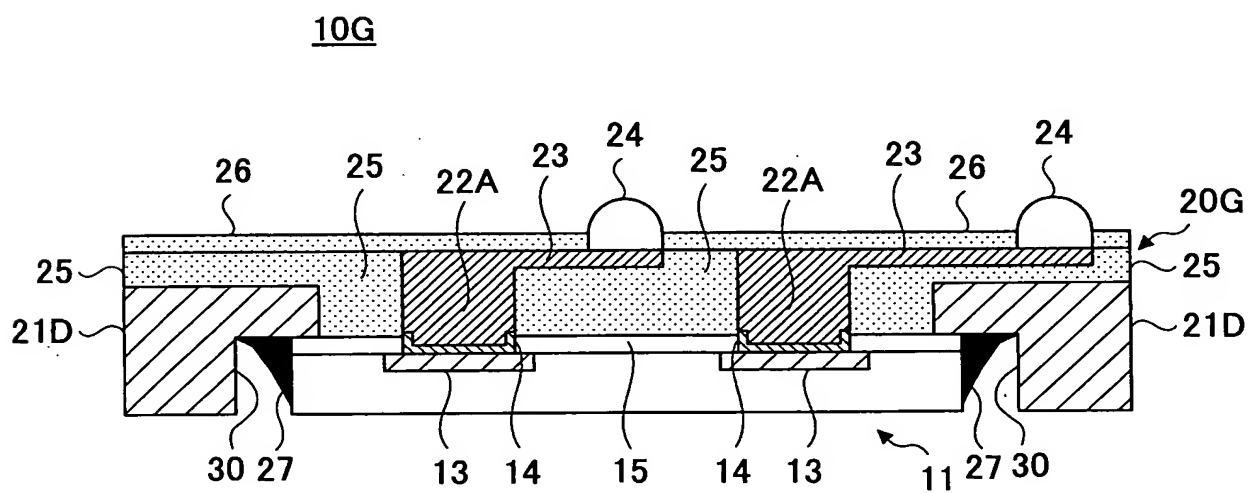


FIG.15

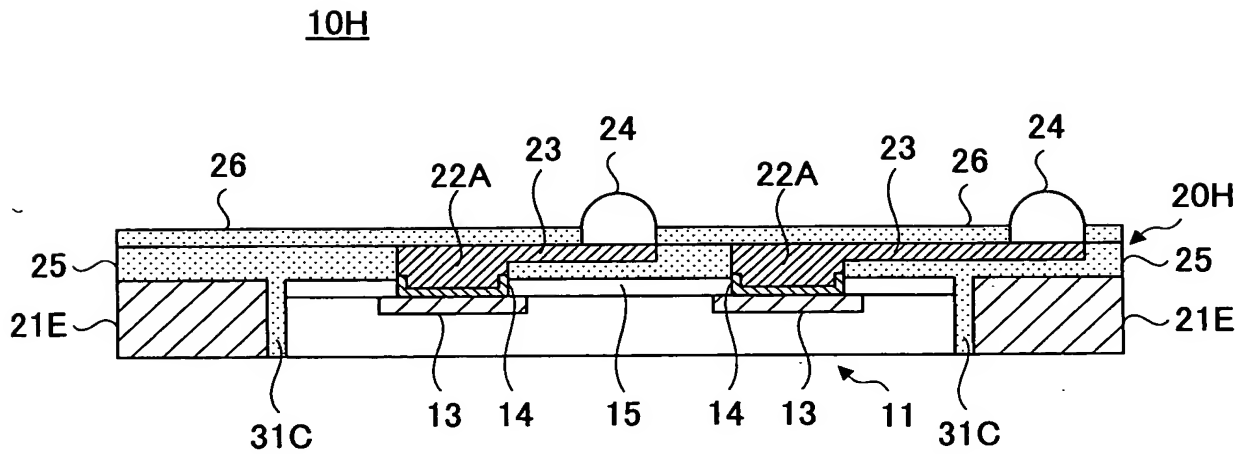


FIG.16

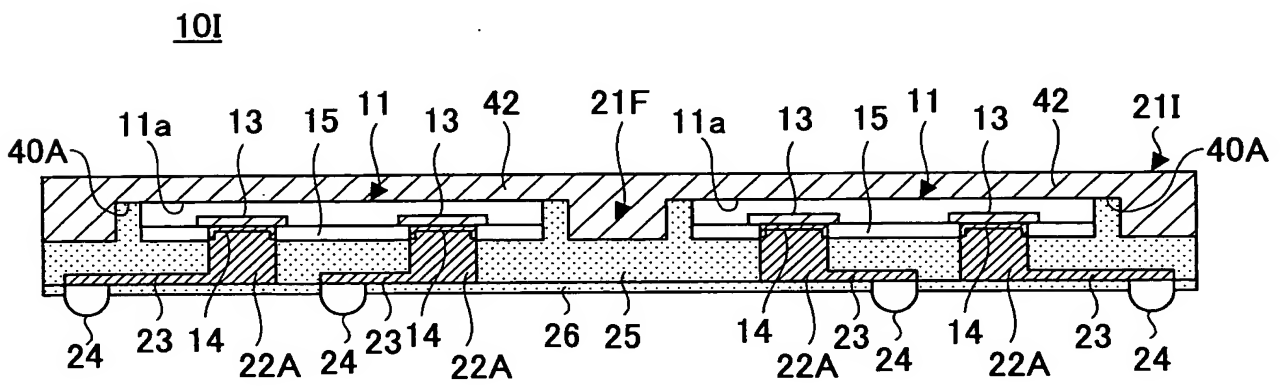


FIG.17

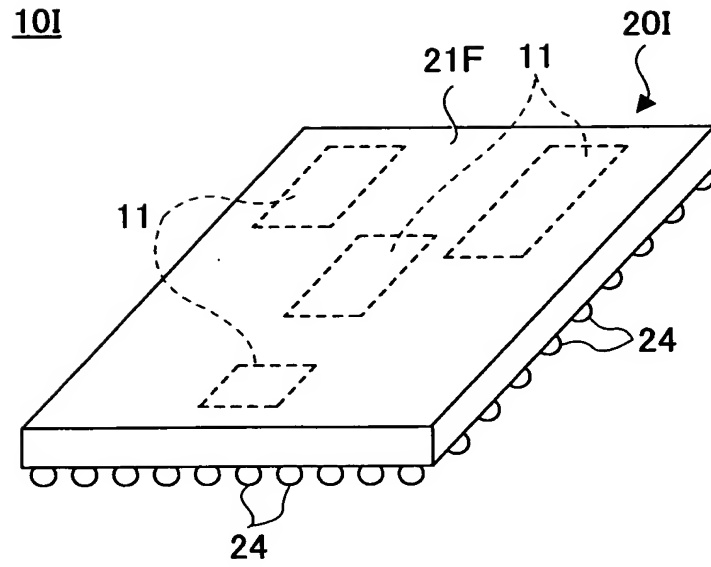


FIG.18

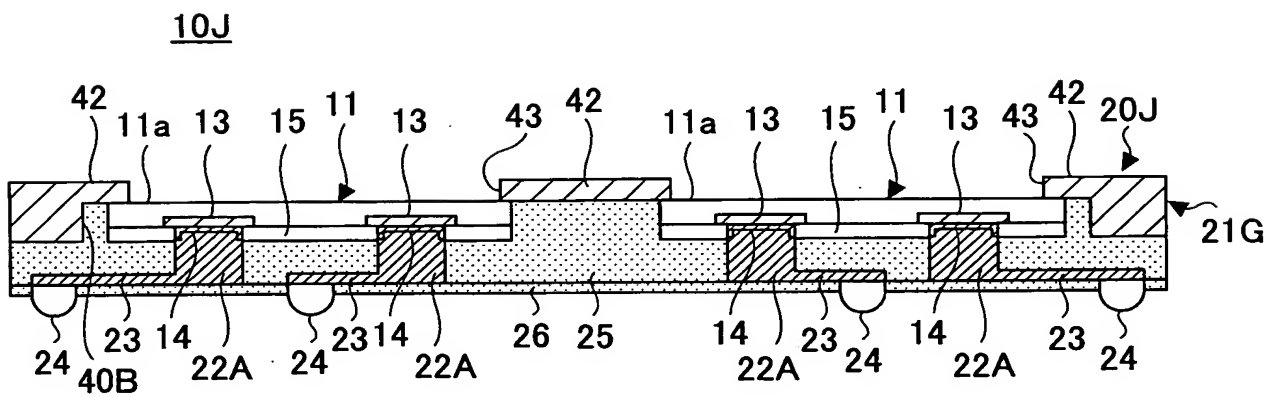


FIG.19

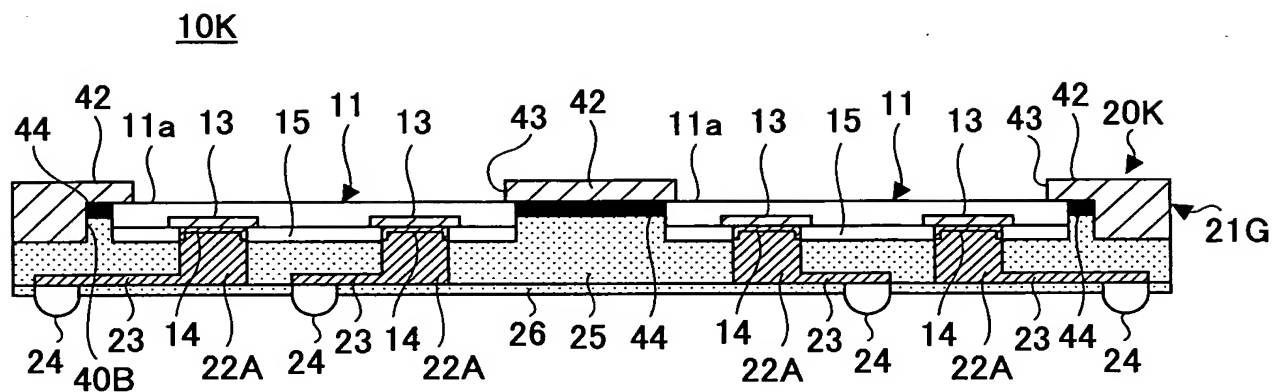


FIG.20

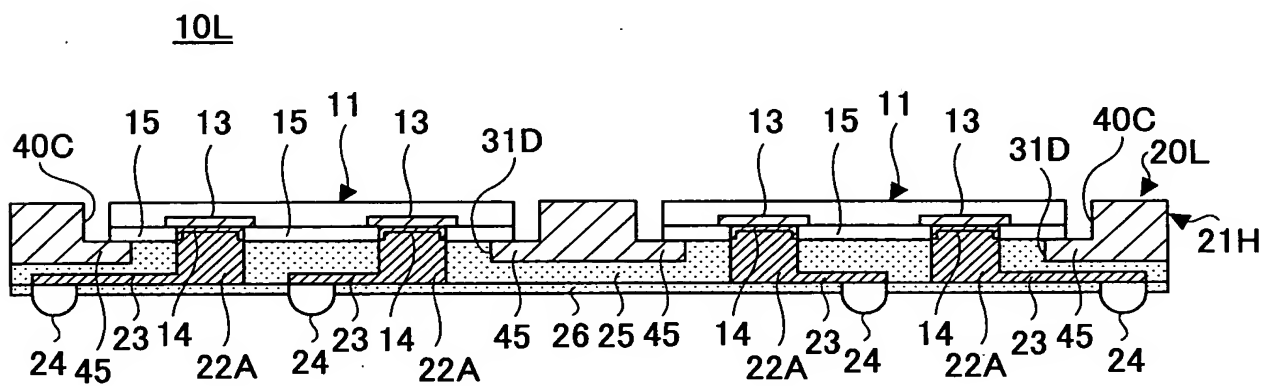


FIG.21

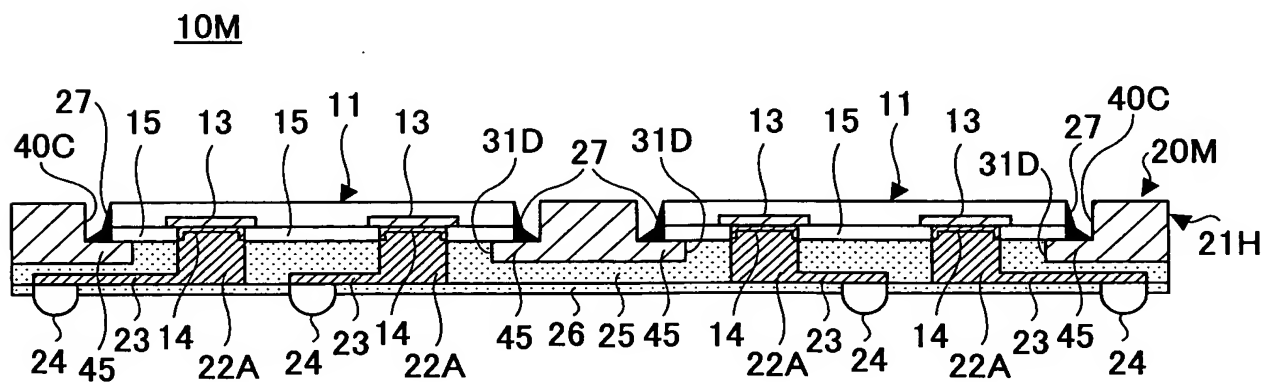


FIG.22

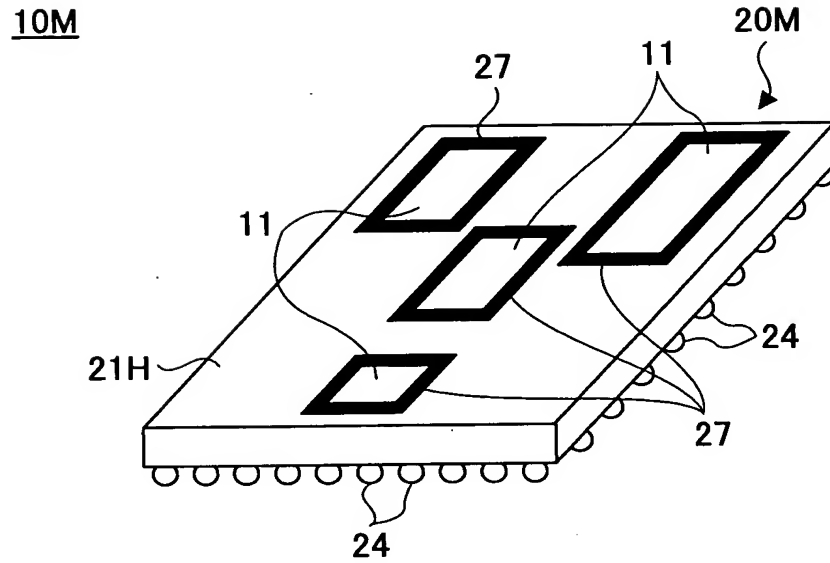


FIG.23

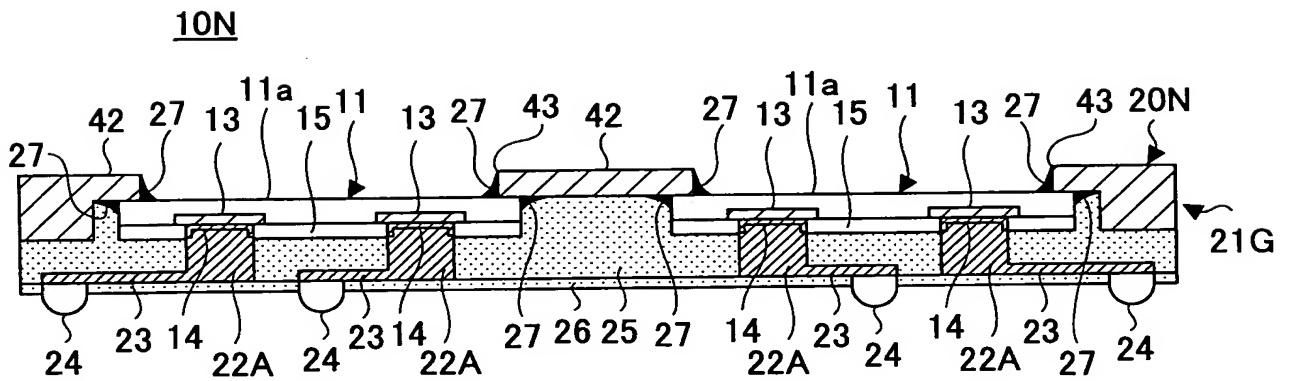


FIG.24

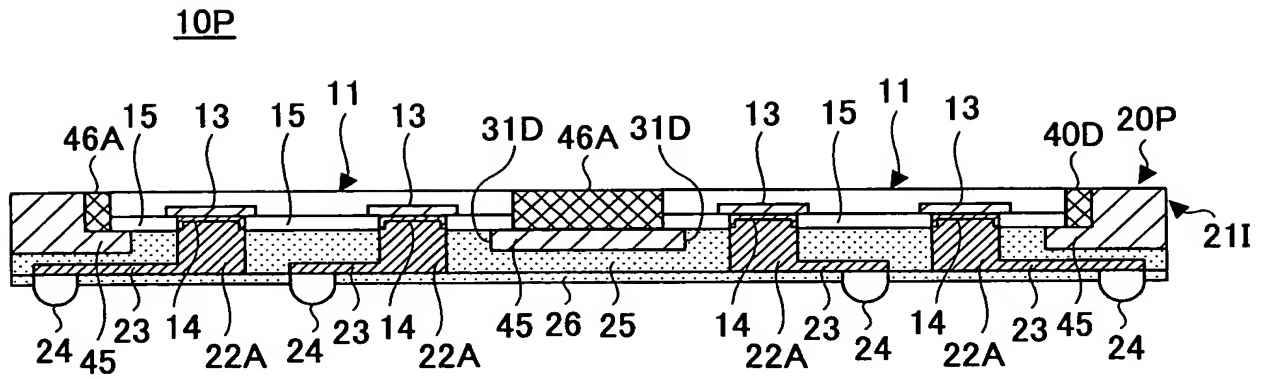


FIG.25

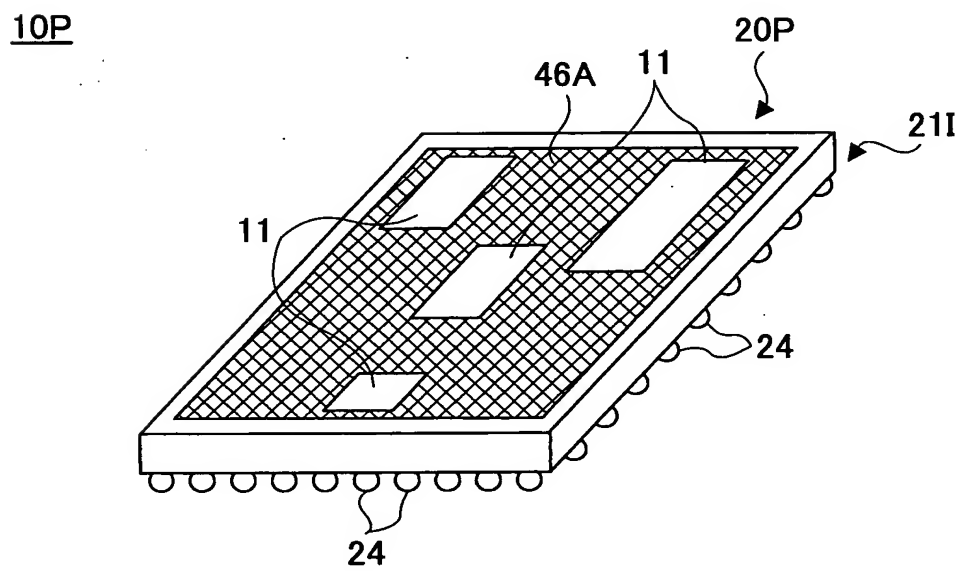


FIG.26

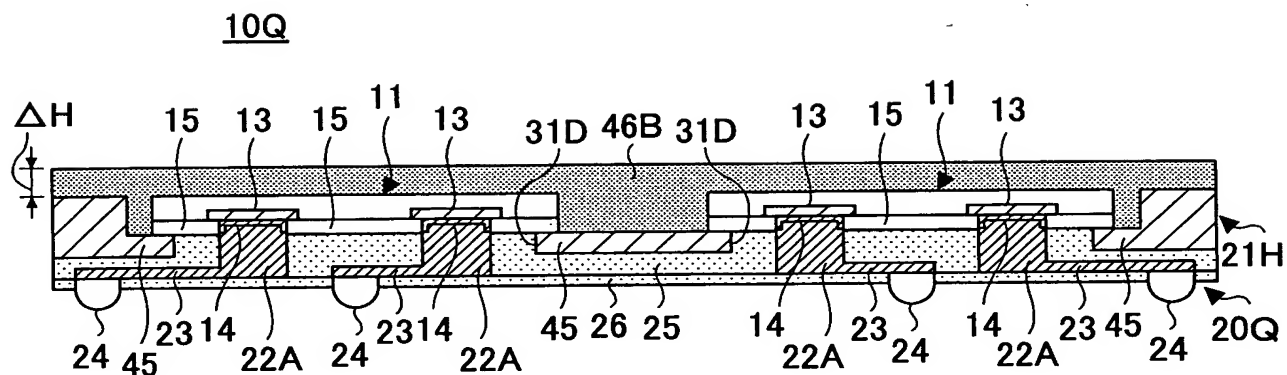


FIG.27

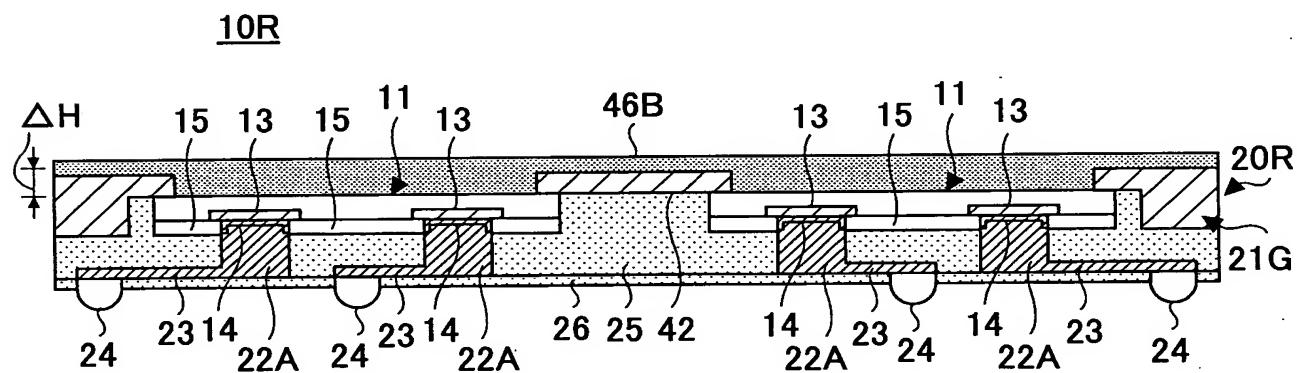


FIG.28

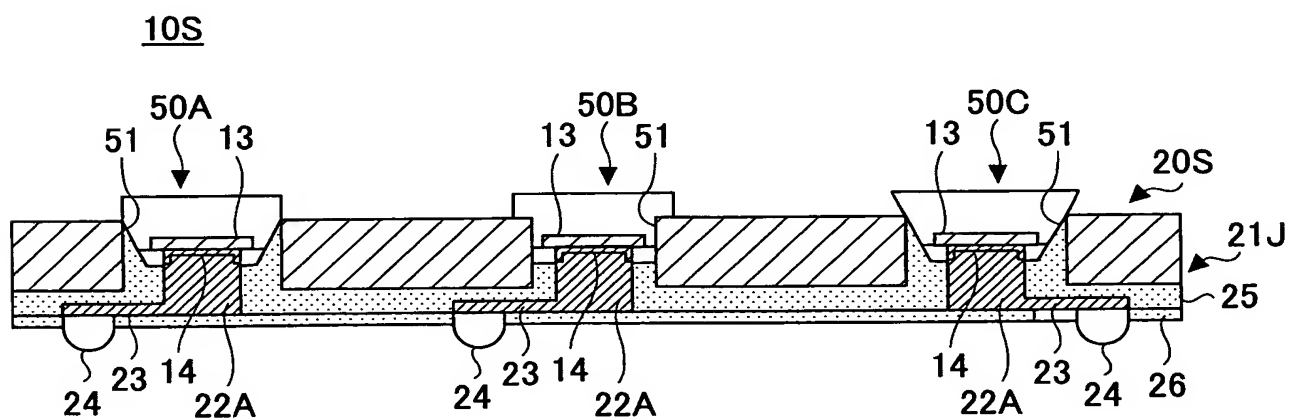


FIG.29

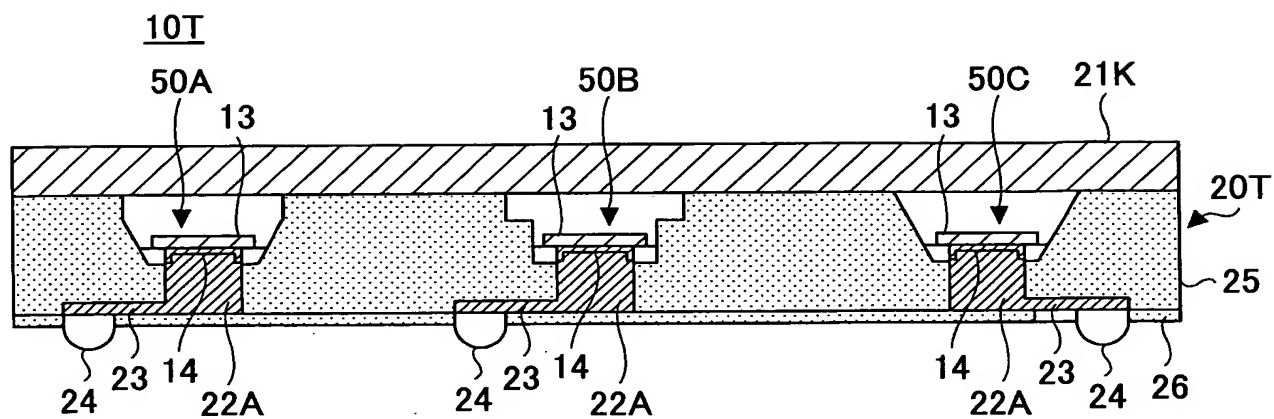


FIG.30

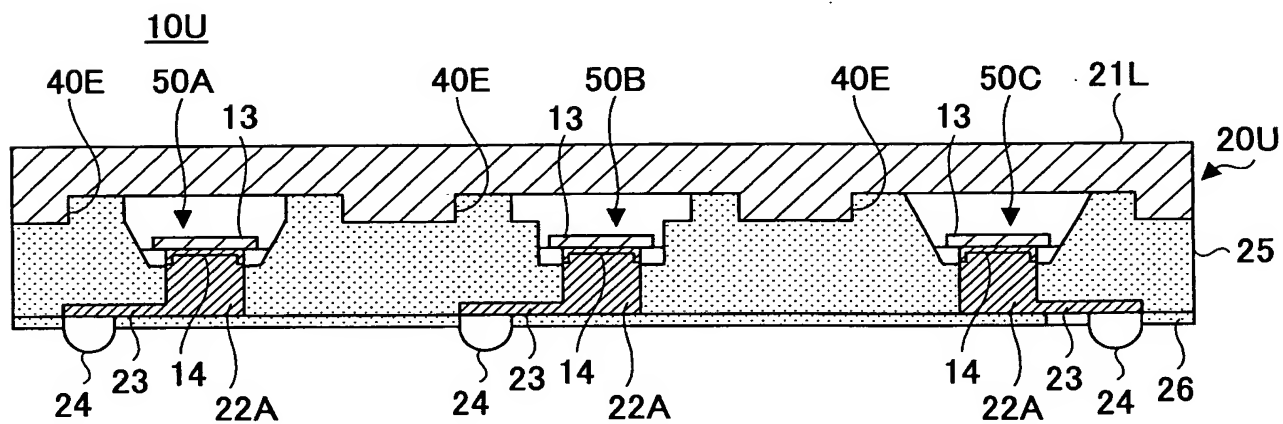


FIG.31

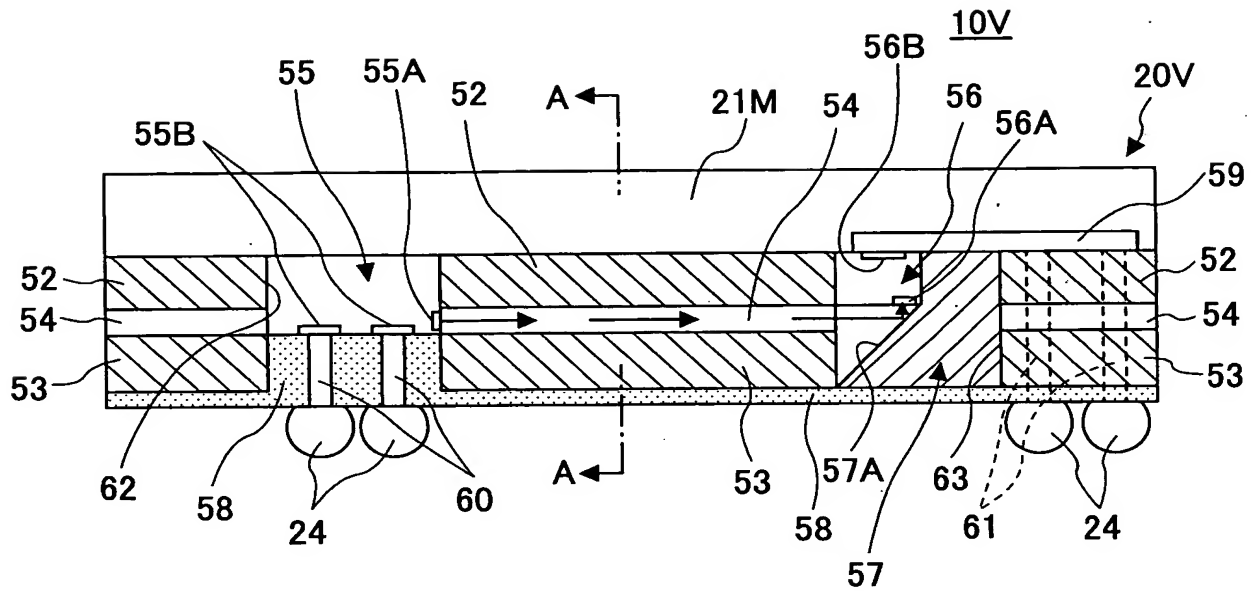


FIG.32

